Form 1449*	Atty. Docket No.: 303.586US1	Serial No. 09/320,421
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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS

**Examiner Initial	(Including Author, Title, Date, Pertinent Pages, Etc.)
KT	Denton, J.P., et al., "Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate", IEEE Electron Device Letters, 17(11), pp. 509-511, (November1996)
KT	Frank, D.J., et al., "Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?", IEDM, pp. 553-556, (1992)
KT	Frank, J., et al., "Monte Carlo Simulations of p- and n-Channel Dual-Gate Si MOSFET's at the Limits of Scaling", IEEE Transactions on Electron Devices, 40(11), pg. 2103, (November 1993)
KT	Mizuno, T., et al., "High Performance Characteristics in Trench Dual-Gate MOSFET (TDMOS)", IEEE Transactions on Electron Devices, 38(9), pp. 2121-2127, (1991)

Examiner [signature] | Date Considered 2/11/02

*Substitute Disclosure Statement Form (PTO-1449)

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